HTM24058A-MIPI

产品名称（**Product name**） : MIPI 接口 TFT 液晶模块

型　　号（**Model**） : HTM24058A-MIPI

编　　号（**Part number**） : 20180824001

日　　期（**Date**） : 2018-8-24

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编码：QR-R-011　A/0　　序号：

Rev	Descriptions	Date
01	Prelimiay Release	2018-8-24

1. Bsaic Specifications

No.	Item	Specification	Unit	Remark
1	LCD Size	2.4”	inch	-
2	Panel Type	a-si TFT	-	-
3	Resolution	240x(3RGB)x320	pixel	-
4	Display Mode	Normally white,Transmissive	-	-
5	Display Number of Colors	262K	-	-
6	Viewing Direction	12 O’clock	-	Note 1
7	Contrast Ratio	170	-	-
8	Luminance	180	cd/m^2	
9	Module Size	43(W)x60.5(L)x3.2 (T)	mm	Note 1
12	Weight	TBD	g	-
13	Driver IC	MIPI-RGB Bridge	-	-
14	Driver IC RAM Size	240x16x320	bit	-
15	Light Source	4 White LEDs in Parallelsss	-	-
16	Interface	MIPI DSI 2-LANS	-	-
17	Operating Temperature	-20~70	℃	-
18	Storage Temperature	-30~80	℃	-

Note 1: Please refer to the mechanical drawing.

2. Pin Assignments

Pin No.	Name	Function
1	BL+	Backlight power supply +3.1V.
2	VDD	Power supply +2.8V.
3	NC	--
4	/RES	Active low reset to the LCM.
5-8	NC	--
9	VSS	Power ground 0V.
10-11	NC	--
12	VSS	Power ground 0V.
13	CLOCKN	Negative differential clock for DSI.
14	CLOCKP	Positive differential clock for DSI.
15	VSS	Power ground 0V.
16	DATAN1	Negative differential data1 for DSI.
17	DATAP1	Positive differential data1 for DSI.
18	BL-	Backlight power ground 0V.
19	DATAN0	Negative differential data0 for DSI.
20	DATAP0	Positive differential data0 for DSI.

3. DSI System Interface

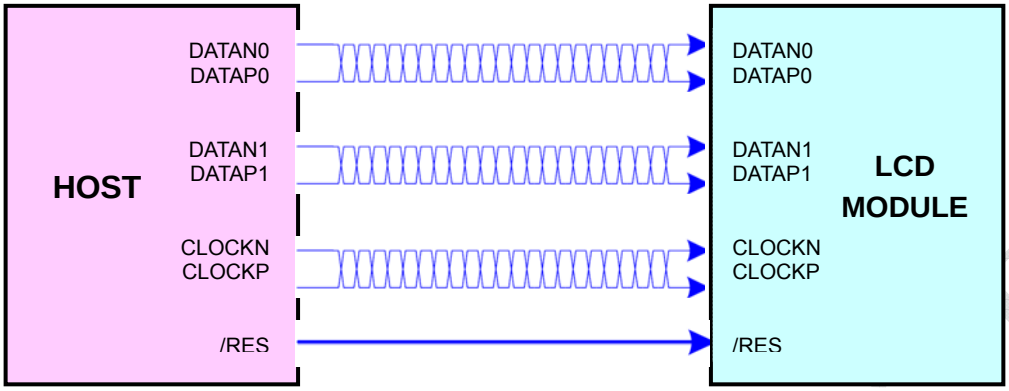


Figure 3-1 DSI System Interface

4. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage	VDD	-0.3	+3.6	V	VSS = 0V
Input Voltage	DSI input	-0.5	1.4	V	VSS = 0V
Operating Temperature	TOP	-20	+70	℃	No Condensation
Storage Temperature	Tst	-30	+80	℃	No Condensation

5. Electrical Characteristics

5.1 DC Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	2.4	2.8	3.3	V
V_{IL}	Low Power logic 1 input voltage	880	-	-	mV
V_{IH}	Low Power logic 0 input voltage	-	-	550	mV
$\|V_{ID}\|$	HS differential input voltage: |Vdp– Vdn|	70	200	270	mV
$\|V_{IDT}\|$	HS differential input voltage threshold	-	-	50	mV
$V_{IL-ULPS}$	Low Power receiver logic 0 voltage, ULP state	-	-	300	mV
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70	-	330	mV
$\triangle V_{CMRX(HF)}$	HS common-mode interference	-	-	100	mV
V_{IHHS}	HS single-ended input high voltage	-	-	460	mV
V_{ILHS}	HS single-ended input low voltage	-40	-	-	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
Z_{ID}	Differential input impedance	80	100	124	Ω

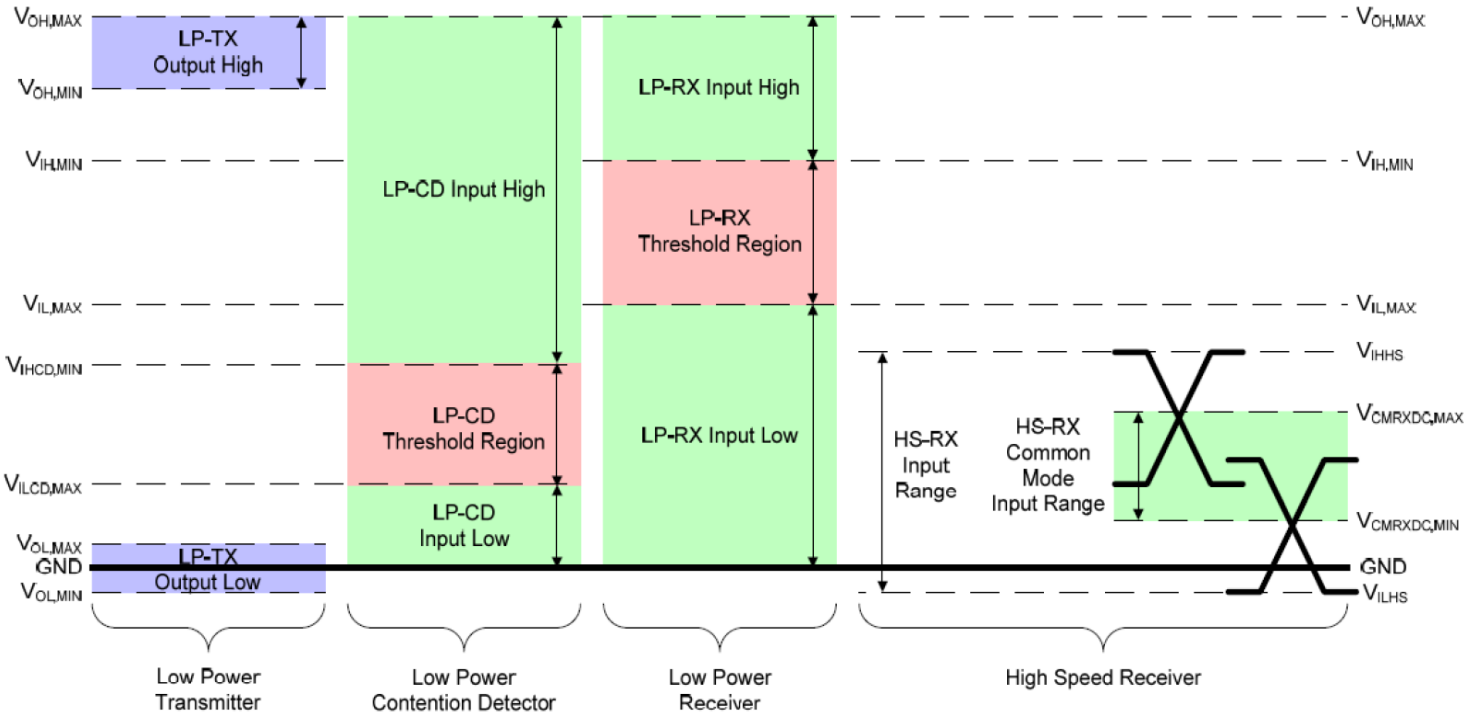


Figure 5-1 DSI signaling and Contention Voltage

5.2 Reset Pin Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
/RES input low level voltage	-	-0.3 V	-	0.3 x VDD	V
/RES input high level voltage	-	0.7 x VDD	-	VDD + 0.3	V
/RES output low level voltage	IOL= 2 mA	-	-	0.5	V
/RES input filtered pulse		-	-	75	ns
/RES input not filtered pulse	-	500	-	-	ns
/RES output pulse	-	20	-	-	μs

5.3 LED Backlight Characteristics

(T_a=+25℃)

Item	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
Current	I_B	-	80	-	mA	Note 1
Power Consumption	P_{BL}	-	240	-	mW	Note 2

Note1: 4 LEDs are connected in parallel; each LED's current consumption is 20mA.

Note2: Where I_B= 120 mA, P_{BL} = I_B x V_{BL}, V_{BL} is backlight forward voltage

6. DSI Transmission Data Format

The LCM receives and interpret 24bpp(RGB888) DSI packets and translates to video stream. Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

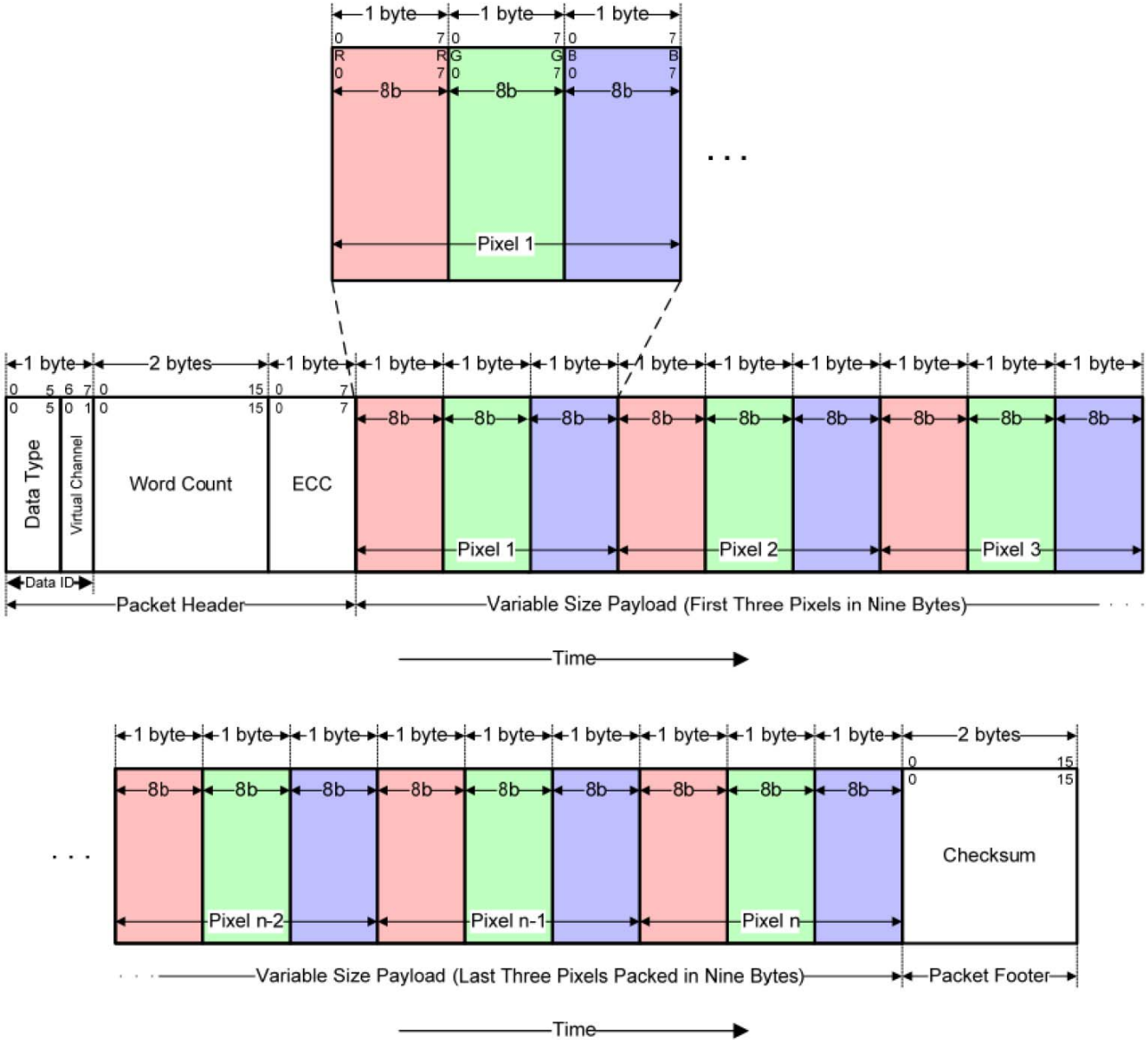


Figure 6-1 DSI RGB888 (24bpp) Color format, Long Packet

7. General DPI Timing

The Pixel clock (DCLK) is running all the time without stopping, it is used for entering VS, HS, DE and DB [23:0] states when there is a rising edge of the DCLK. The DCLK can not be used as the internal clock for other functions of the display module.

Vertical synchronization (Vsync) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DCLK signal.

DE (Data Enable) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DCLK signal. DB[23:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DCLK). DB [23:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DCLK signal.

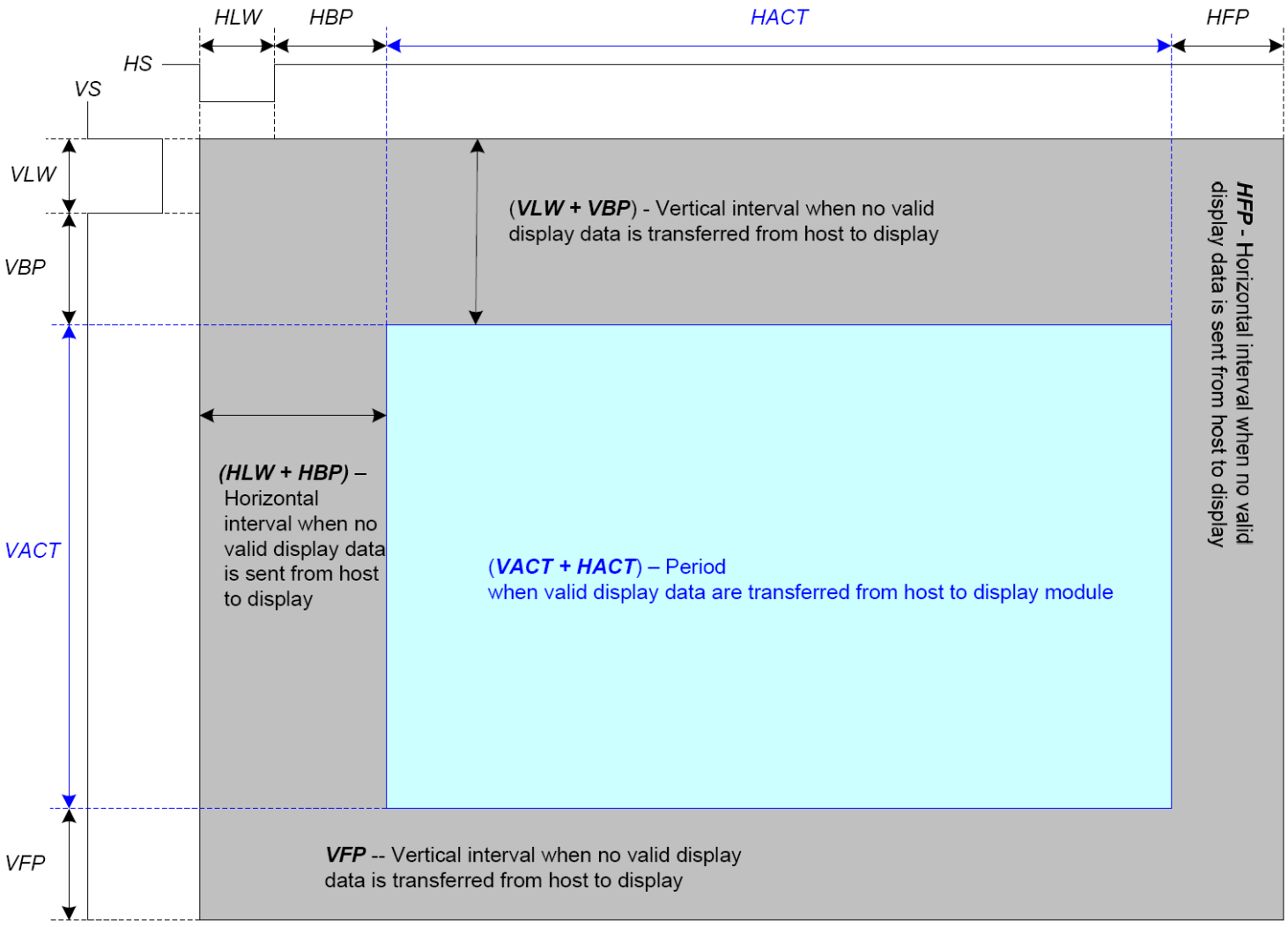


Figure 7-1 DRAM Access Area by RGB Interface

8. DPI Interface Timing

The timing chart of 24-bit DPI (RGB) interface mode is illustrated in Figure 6-1.

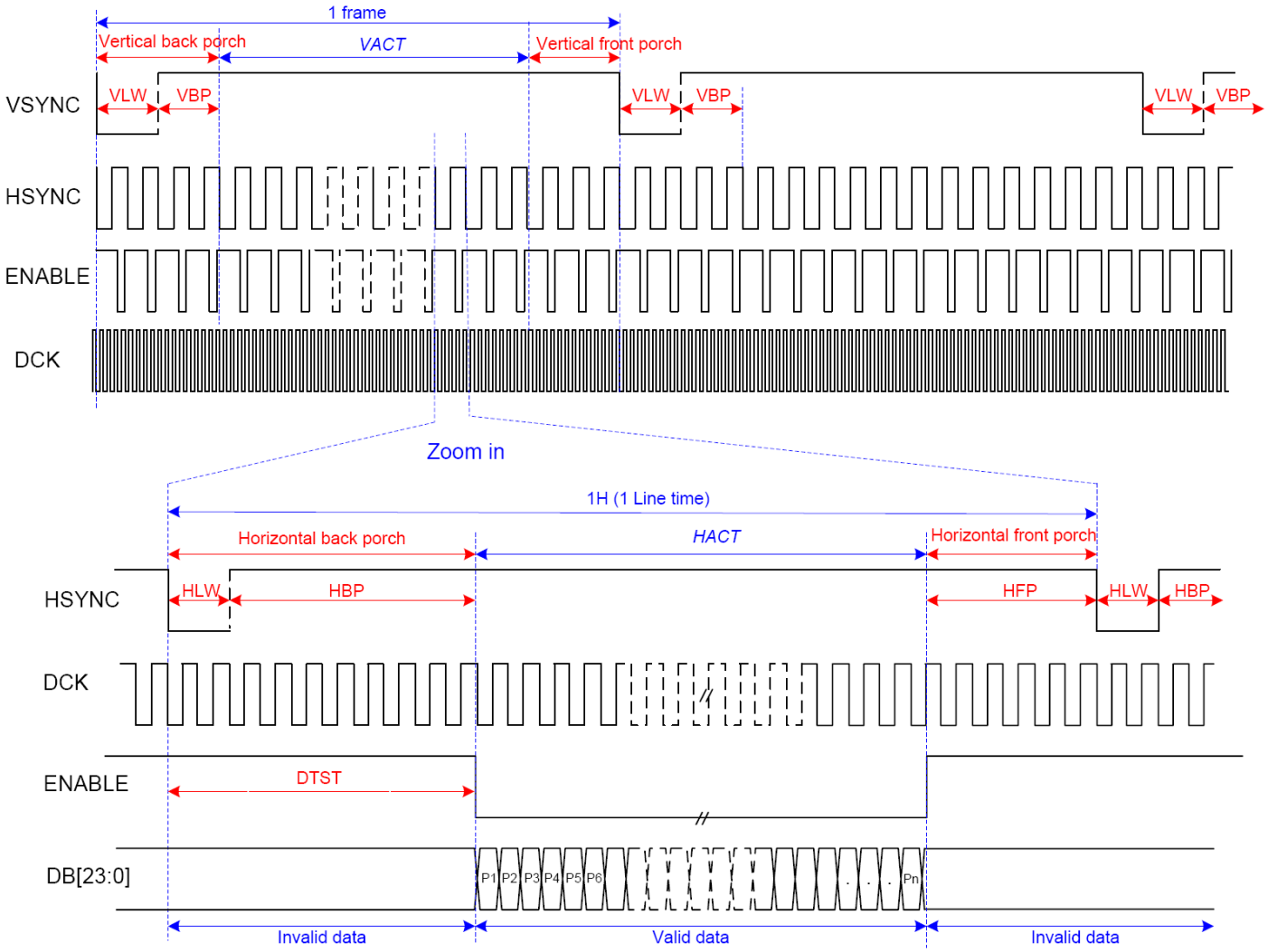


Figure 8-1 DPI Interface Timing

Note :
VLW -- VSYNC Low pulse Width
HLW -- HSYNC Low pulse Width
DTST -- Data Transfer Startup Time
Pn -- pixel 1, pixel 2…, pixel n.

Parameter	Symbols	Min.	Typ.	Max.	Units
Frame Rate	FR	50	68	80	fps
Dots Clock Frequency	DCLK	-	7	-	MHz
Horizontal Address	HACT	-	240	-	DCLK
Horizontal Front Porch	HFP	2	38	-	DCLK
Horizontal Low Pulse width	HLW	2	10	HLW+ HBP=31	DCLK
Horizontal Back Porch	HBP	4	10	HLW+ HBP=31	DCLK
Vertical Address	VACT	-	320	-	Line
Vertical Front Porch	VFP	1	8	-	Line
Vertical Low Pulse width	VLW	1	4	VLW+ VBP=127	Line
Vertical Back Porch	VBP	1	20	VLW+ VBP=127	Line

Note: DCLK=FRx(VLW+VACT+VBP)x(HLW+HACT+HBP+HFP)

9. DSI Video Transmission Sequence

The LCM supports Non-Burst Mode with Sync Pulses, Non-Burst Mode with Sync Events and Burst mode.

9.1 Non-Burst Mode with Sync Pulses:

Enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.

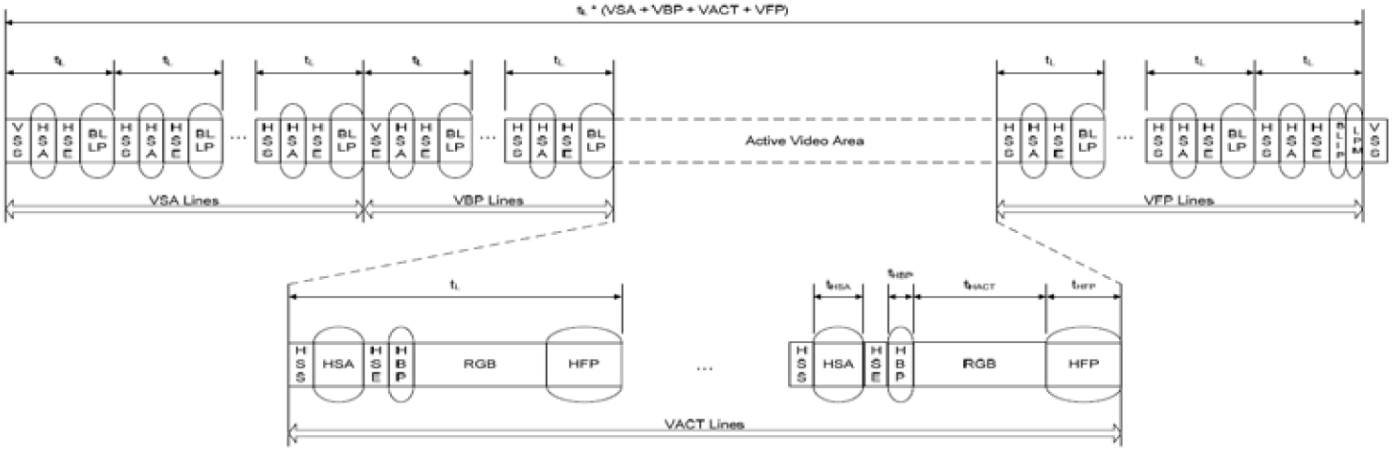


Figure 9-1 Non-Burst Mode with Sync Pulses

9.2 Non-Burst Mode with Sync Events:

Similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.

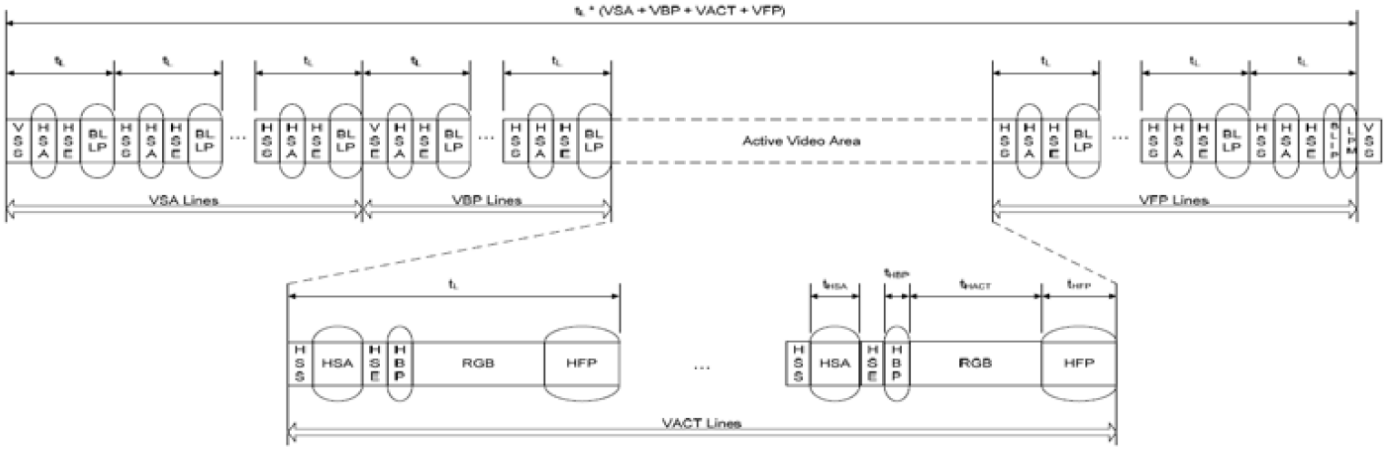


Figure 9-2 Non-Burst Mode with Sync Events

9.3 Burst mode:

The RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode(saving power).

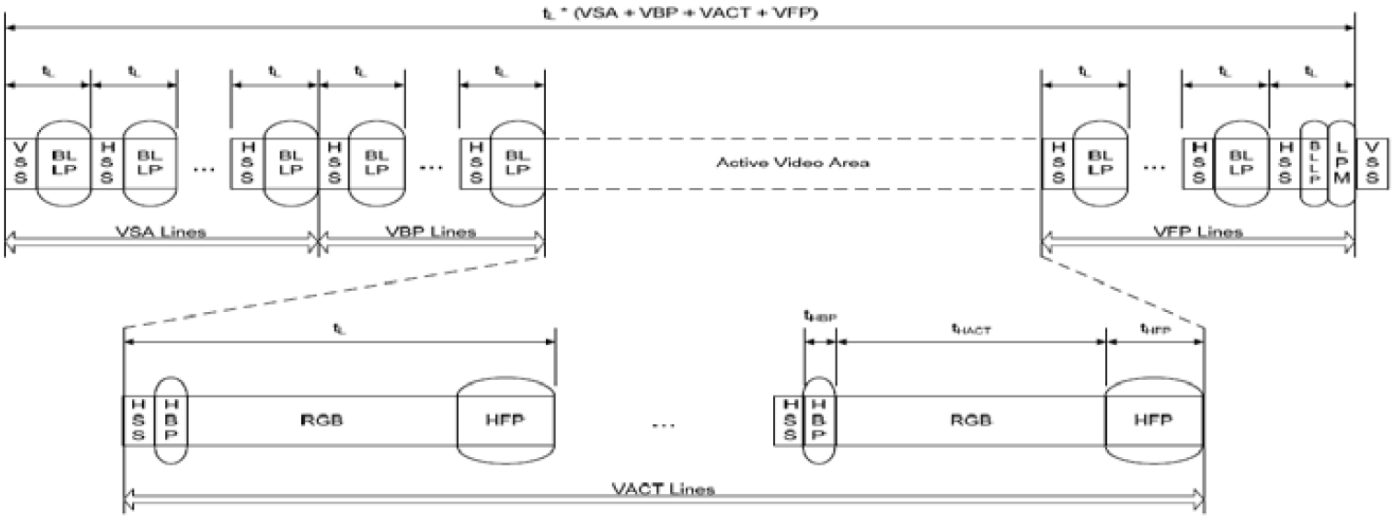


Figure 9-3 Burst mode

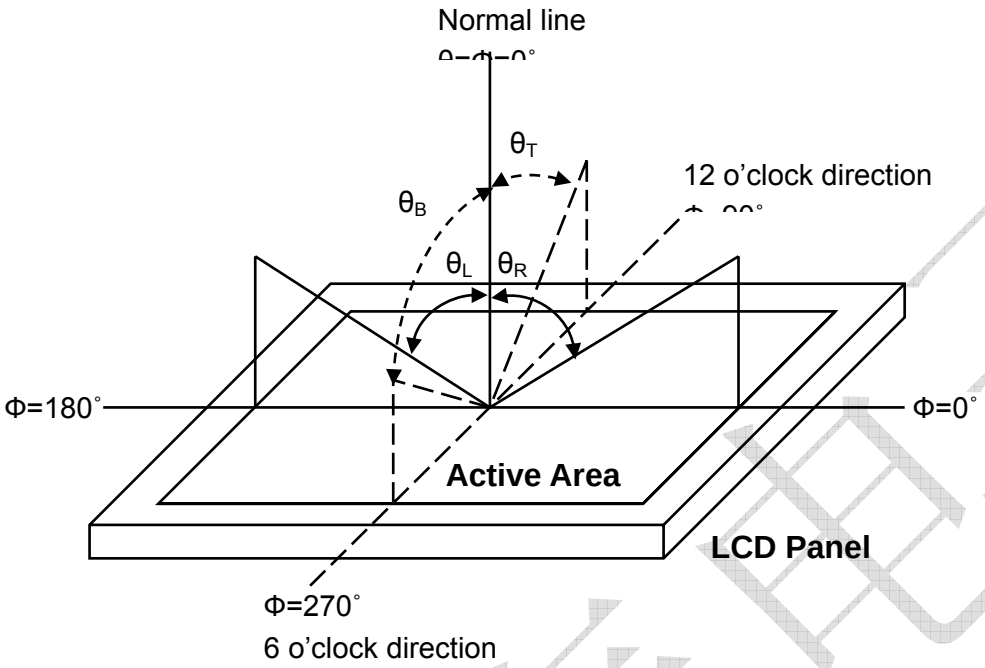
For all three sequences, the first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, the LVDS output video timing(HS-Horizontal sync and VS-Vertical sync) are generated based on the synchronization.

10. Optical Specifications

(T_a=+25℃, VCI=2.8V, VDD=1.8V, I_B=46mA)

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	CR≧10	—	45	-	degree	Note 1,2
	Right	θ_R		—	45	-		
	Top	θ_T		—	50	-		
	Bottom	θ_B		—	20	-		
Response Time		T_{on} +T_{off}	Normal θ=Φ=0°	-	30	50	ms	Note 2,3
Contrast Ratio		CR	Normal θ=Φ=0°	200	300	-	-	Note 2,4
Luminance		L	Normal θ=Φ=0°	160	200	-	cd/m^2	Note 2,5
Flicker		-	-	No Visible			-	Note 8
Crosstalk		-	-	No Visible			-	Note 9
Color Chromaticity (CIE1931)	White	W_x	Normal θ=Φ=0°	—	0.30	—	-	Note 2,6
		W_y		—	0.31	—		
	Red	R_x			0.59	—		
		R_y		—	0.32	—		
	Green	G_x		—	0.31	—		
		G_y		—	0.56	—		
	Blue	B_x		—	0.15	—		
		B_y		—	0.08	—		
Color Gamut		NTSC	CIE1931	-	58	-	%	-
Luminance Uniformity		U_L	Normal θ=Φ=0°	—	80	-	%	Note 2,7

Note 1: Definition of viewing angle



range

Fig. 1 Definition of viewing angle

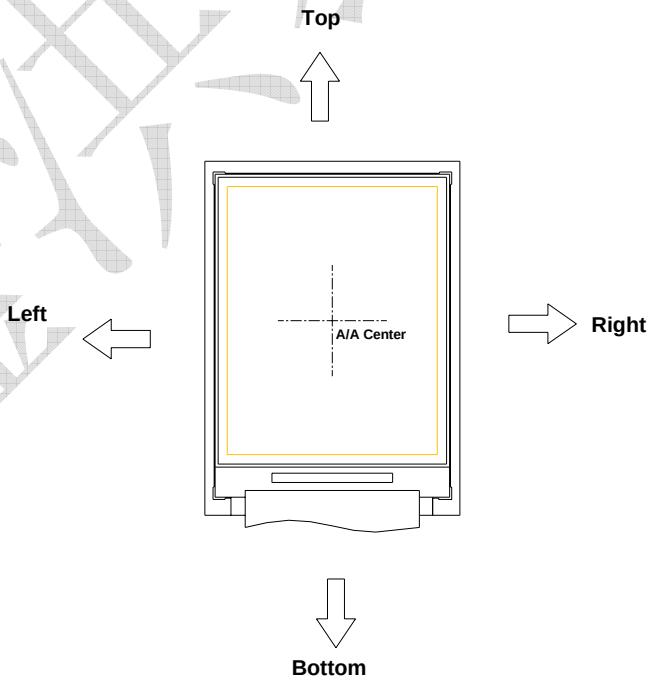


Fig. 2 Definition of viewing angle for display

Note 2: Definition of optical measurement system

The optical characteristics should be measured in a dark room with ambient temperature T_a=+25.The optical properties are measured at the center point of the LCD screen after 5 minutes operation. (Equipment: Photo detector TOPCON BM-5A or BM-7 /Field of view: 1˚ /Height: 500mm.)

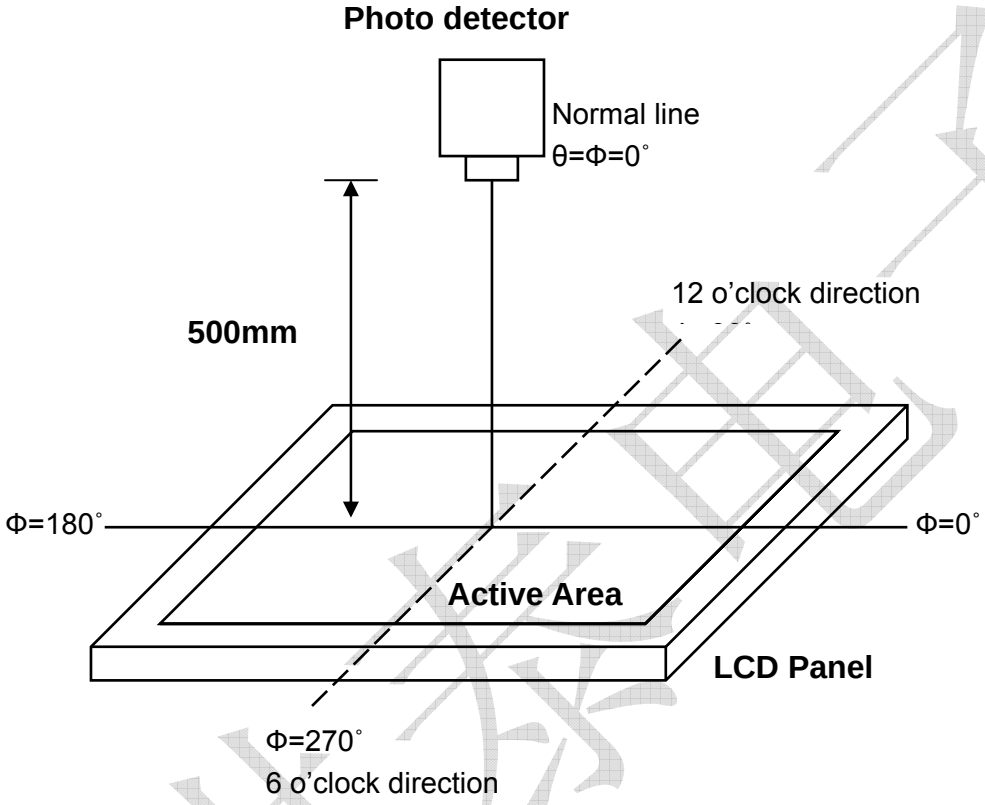


Fig. 10-1 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.

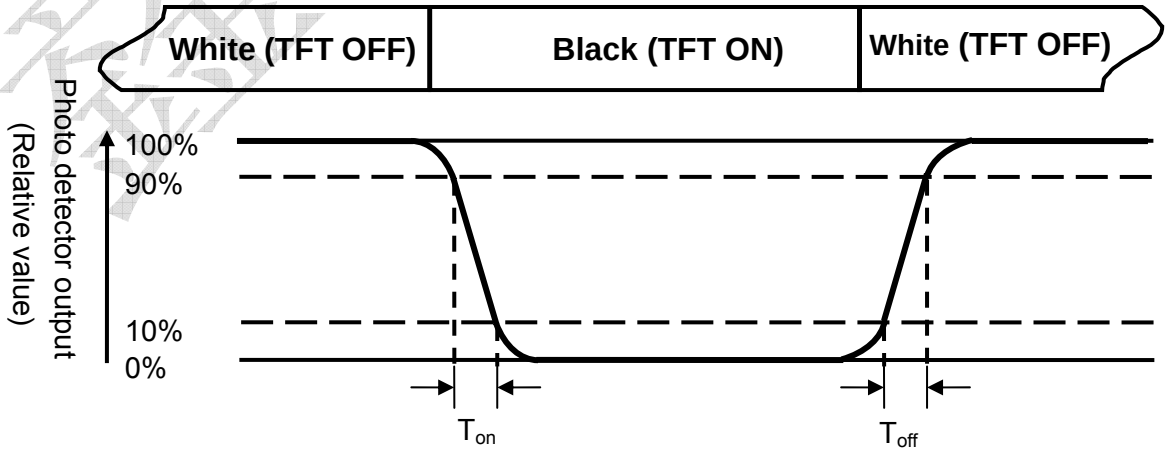


Fig. 10-2 Definition of response timeNote 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity } (U_L) = \frac{L_{min}}{L_{max}}$$

L-------Active area length W----- Active area width

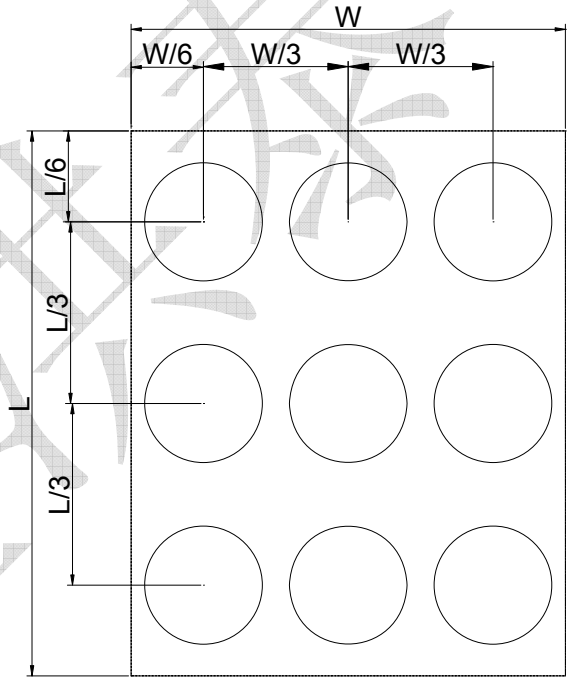


Fig. 10-3 Definition of luminance uniformity

L_{max} : The measured maximum luminance of all measurement position.

L_{min} : The measured minimum luminance of all measurement position.

Note 8: Definition of Flicker

Flicker is the pattern usually used to describe the visual sensation produced by a rapidly varying light intensity. There should be no visible flicker in normal direction of the display when the following figure are loaded.

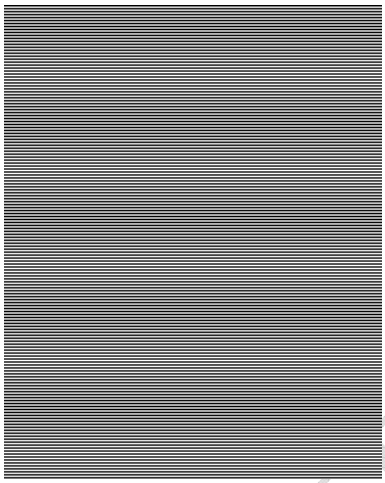


Fig.10-4 Flicker checker pattern

Note9: Definition of crosstalk

There should be no visible in normal direction of the display when the following figures are loaded.

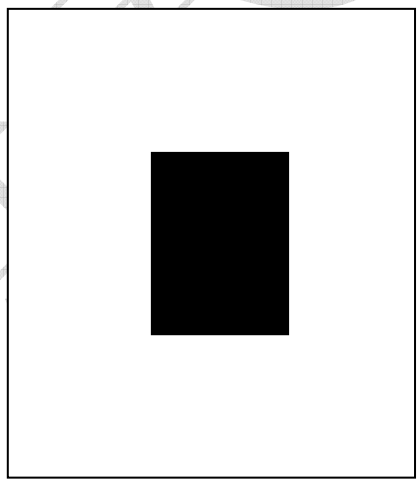


Fig.10-5 Crosstalk checker pattern

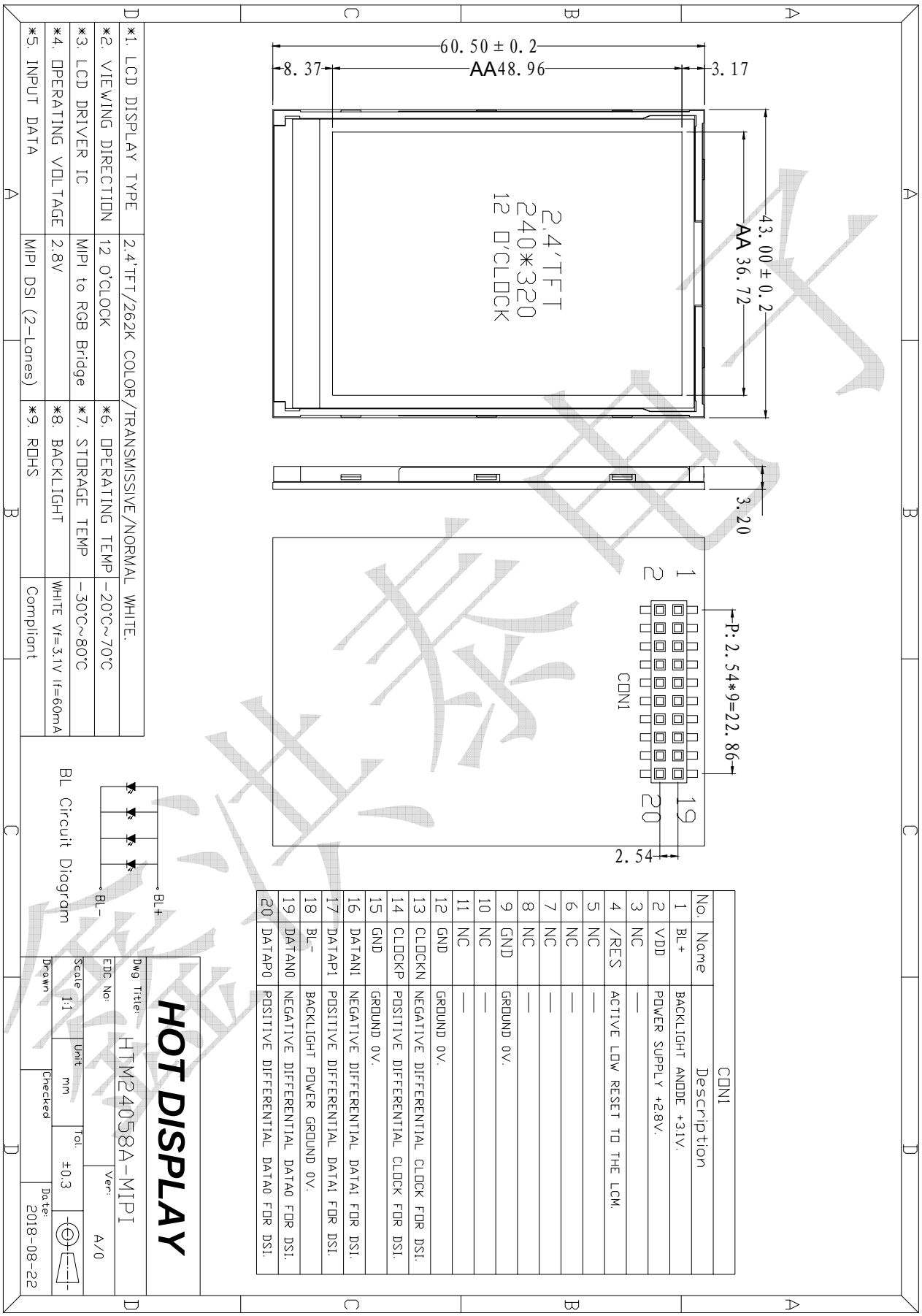
11. Reliability Test Items

Test Items	Test Conditions	Remark
High Temperature Storage	+80℃±3℃ for 240 hours	-
Low Temperature Storage	-30℃±3℃ for 240 hours	-
High Temperature Operation	+70℃±3℃ for 240 hours	-
Low Temperature Operation	-20℃±3℃ for 240 hours	-
High Temperature and Humidity Operation	+60℃±3℃, 90%±3%RH max. for 240 hours	-
Thermal Shock	-30℃/0.5h ~ +80℃/0.5h for a total 100 cycles, Start with cold temp and end with high temp	-
Vibration Test	Frequency range:10~55Hz Stoke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X. Y. Z. (6 hours for total)	-
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	-
Package Vibration Test	Random Vibration : $0.015G^2$/Hz from 5-200Hz, -6dB/Octave from 200-500Hz 1 hour for each direction of X. Y. Z. (3 hours for total)	-
Package Drop Test	Height :76cm(Weight≦10kg); 60cm(Weight>10kg) 1 corner, 3 edges, 6 surfaces	-
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	-

Note1: During the display practical test under normal operation condition, there shall be no change, which may affect display function.

Note2: Before functional check, the test sample requires a 2 hours storage time at room temperature

12. Mechanical Drawing



∗1. LCD DISPLAY TYPE	2.4'TFT/262K COLOR/TRANSMISSIVE/NORMAL WHITE.	
∗2. VIEWING DIRECTION	12 O'CLOCK	∗6. OPERATING TEMP -20°C~70°C
∗3. LCD DRIVER IC	MIPI to RGB Bridge	∗7. STORAGE TEMP -30°C~80°C
∗4. OPERATING VOLTAGE	2.8V	∗8. BACKLIGHT WHITE Vf=3.1V If=60mA
∗5. INPUT DATA	MIPI DSI (2-Lanes)	∗9. ROHS Compliant

CON1

No.	Name	Description
1	BL+	BACKLIGHT ANODE +31V.
2	VDD	POWER SUPPLY +2.8V.
3	NC	—
4	/RES	ACTIVE LOW RESET TO THE LCM.
5	NC	—
6	NC	—
7	NC	—
8	NC	—
9	GND	GROUND 0V.
10	NC	—
11	NC	—
12	GND	GROUND 0V.
13	CLOCKN	NEGATIVE DIFFERENTIAL CLOCK FOR DSI.
14	CLOCKP	POSITIVE DIFFERENTIAL CLOCK FOR DSI.
15	GND	GROUND 0V.
16	DATAN1	NEGATIVE DIFFERENTIAL DATA1 FOR DSI.
17	DATAP1	POSITIVE DIFFERENTIAL DATA1 FOR DSI.
18	BL-	BACKLIGHT POWER GROUND 0V.
19	DATAN0	NEGATIVE DIFFERENTIAL DATA0 FOR DSI.
20	DATAP0	POSITIVE DIFFERENTIAL DATA0 FOR DSI.